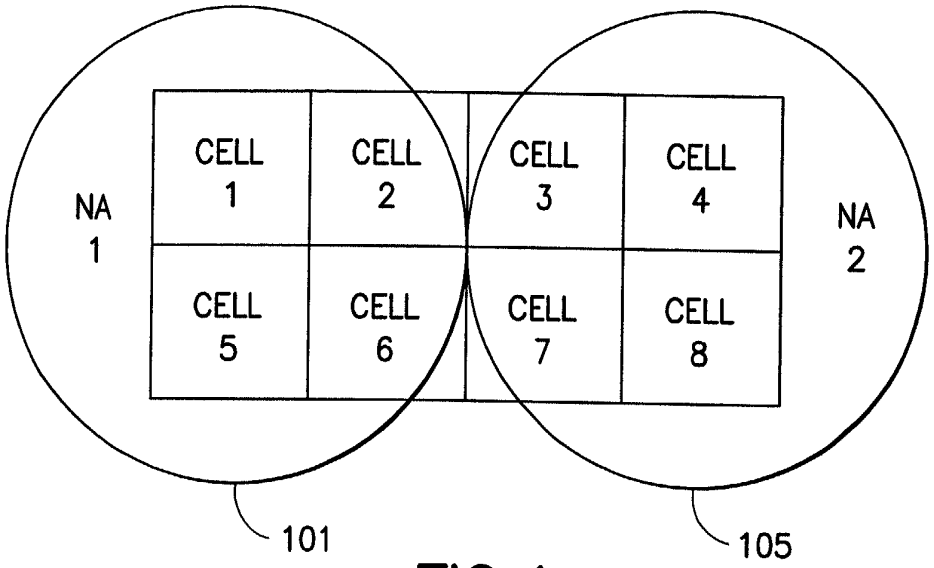
NA
1
CELL
1
CELL
2
CELL
3
CELL
4
CELL
5
CELL
6
CELL
7
CELL
8
NA
2
101
105

FIG. 1

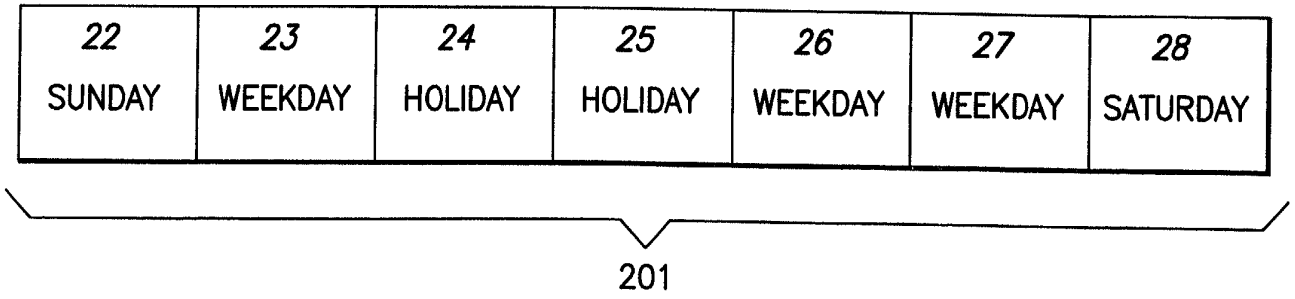
22
SUNDAY
23
WEEKDAY
24
HOLIDAY
25
HOLIDAY
26
WEEKDAY
27
WEEKDAY
28
SATURDAY
201

FIG. 2

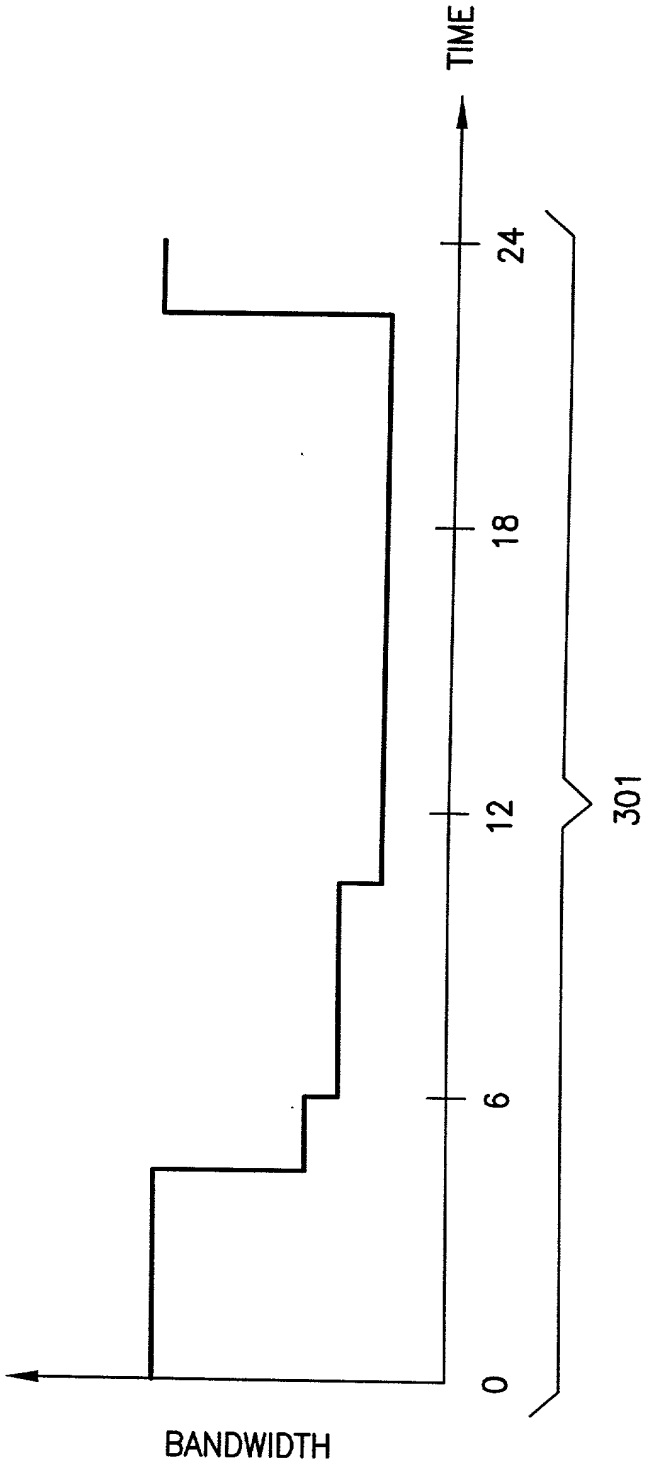

FIG.3

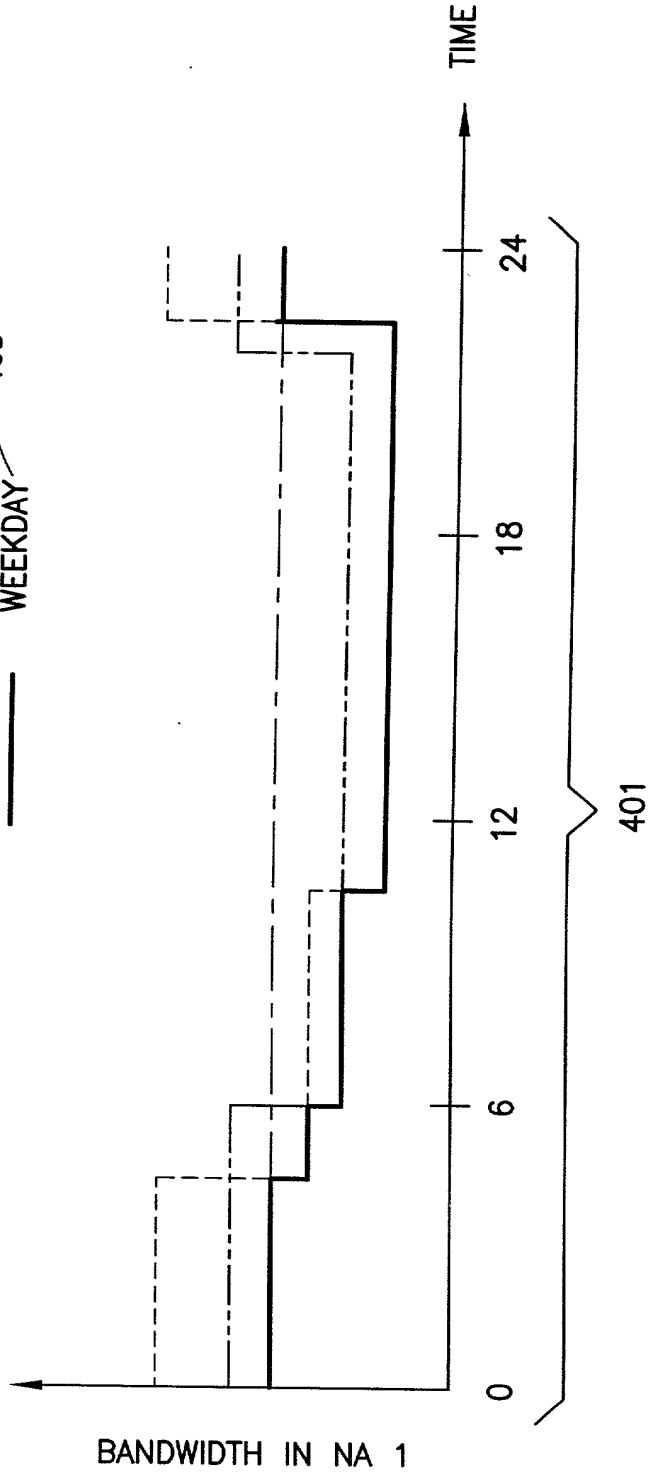
TIME
24
18
12
6
0
401
403
3.1.01
405
5.6.01
407
31.12.01
409
WEEKDAY
BANDWIDTH IN NA 1

FIG.4

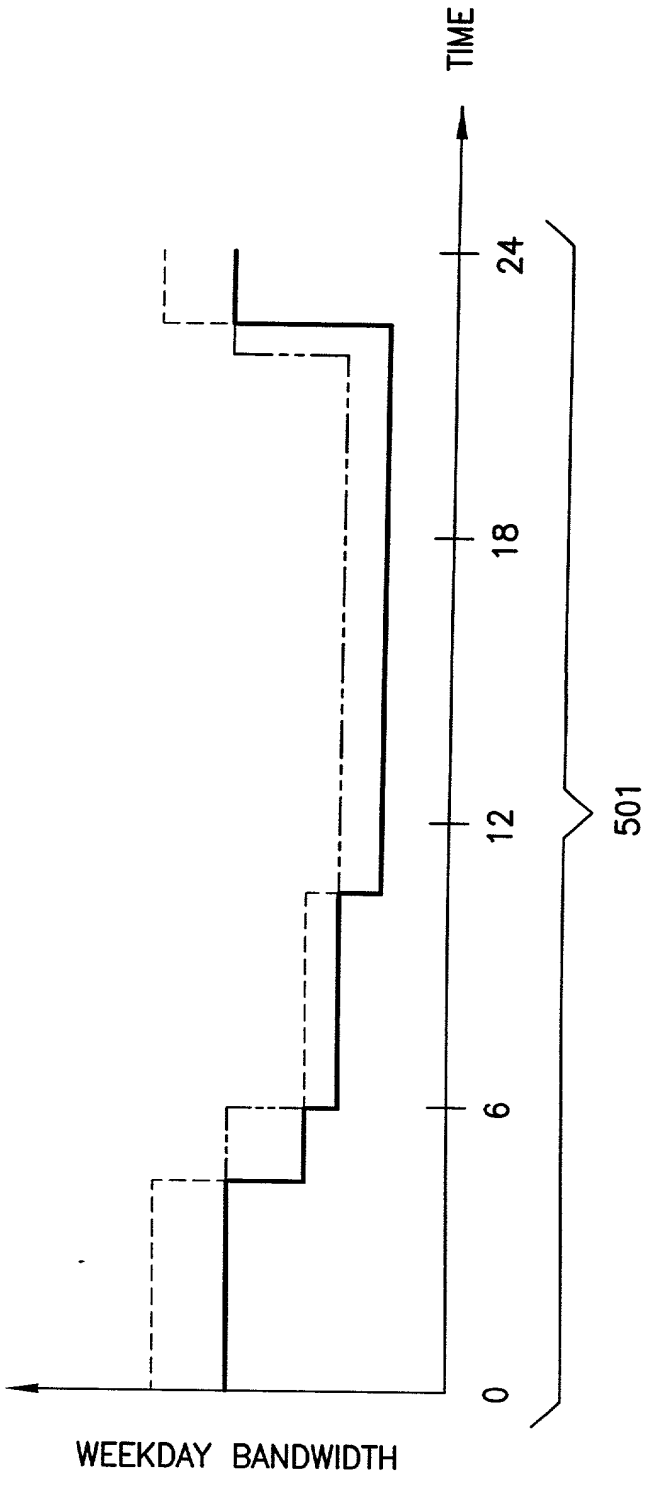
TIME
24
18
12
6
0
501
WEEKDAY BANDWIDTH
NA 1
507
NA 2
505
GLOBAL
503

FIG.5

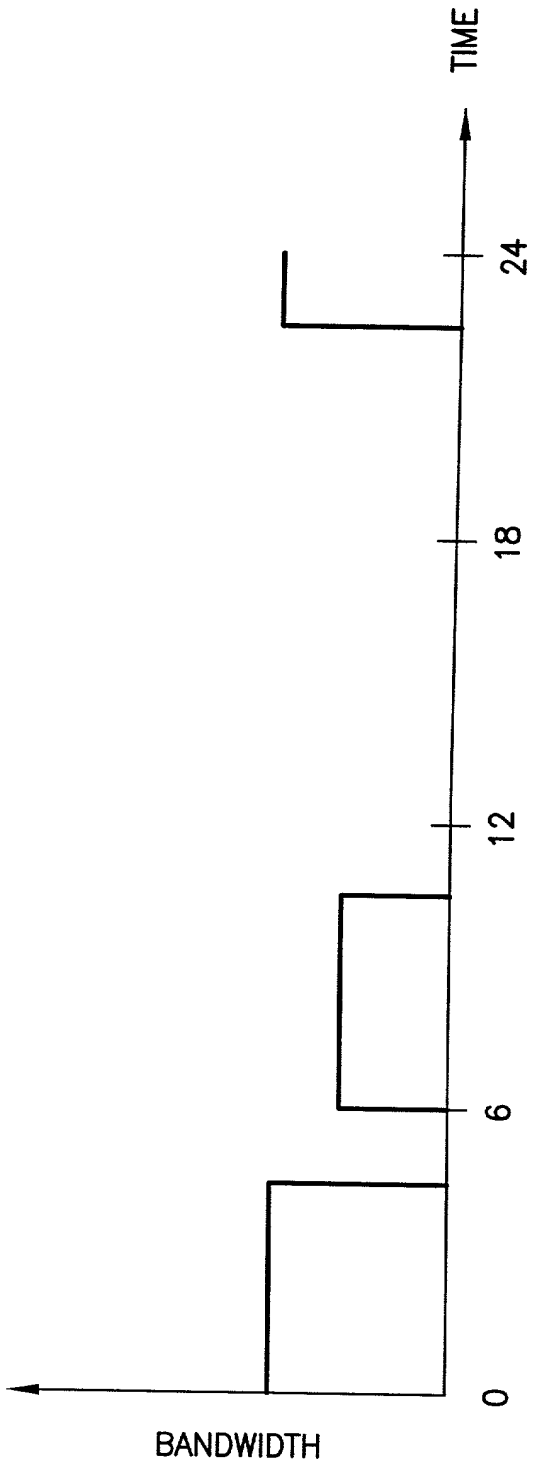

FIG.6

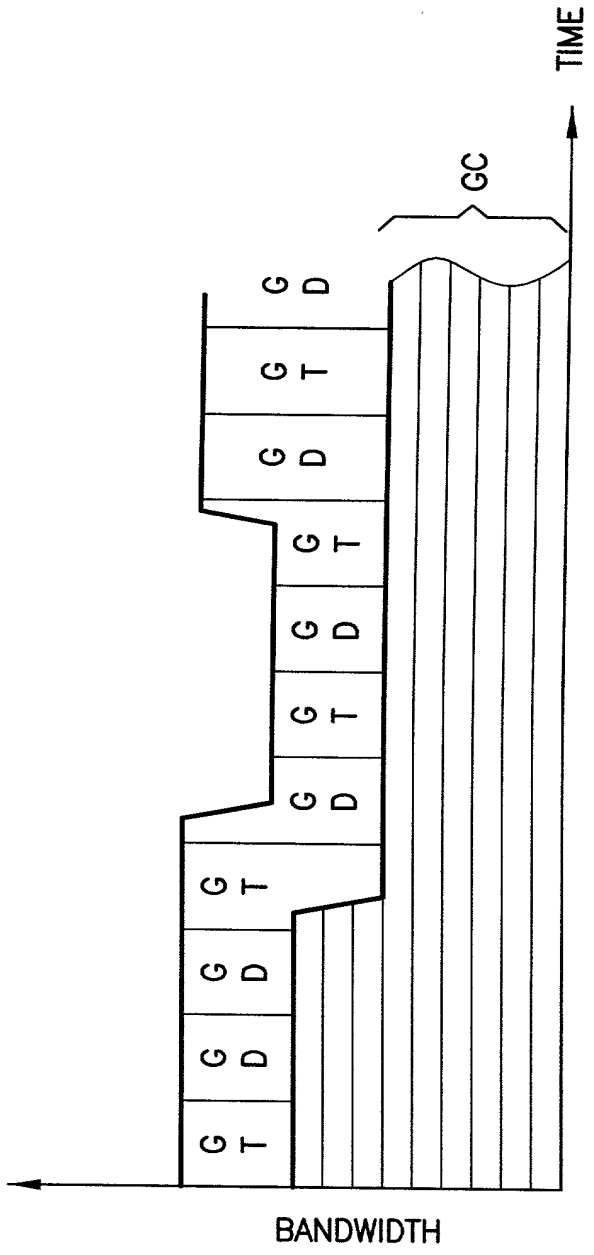

FIG.7

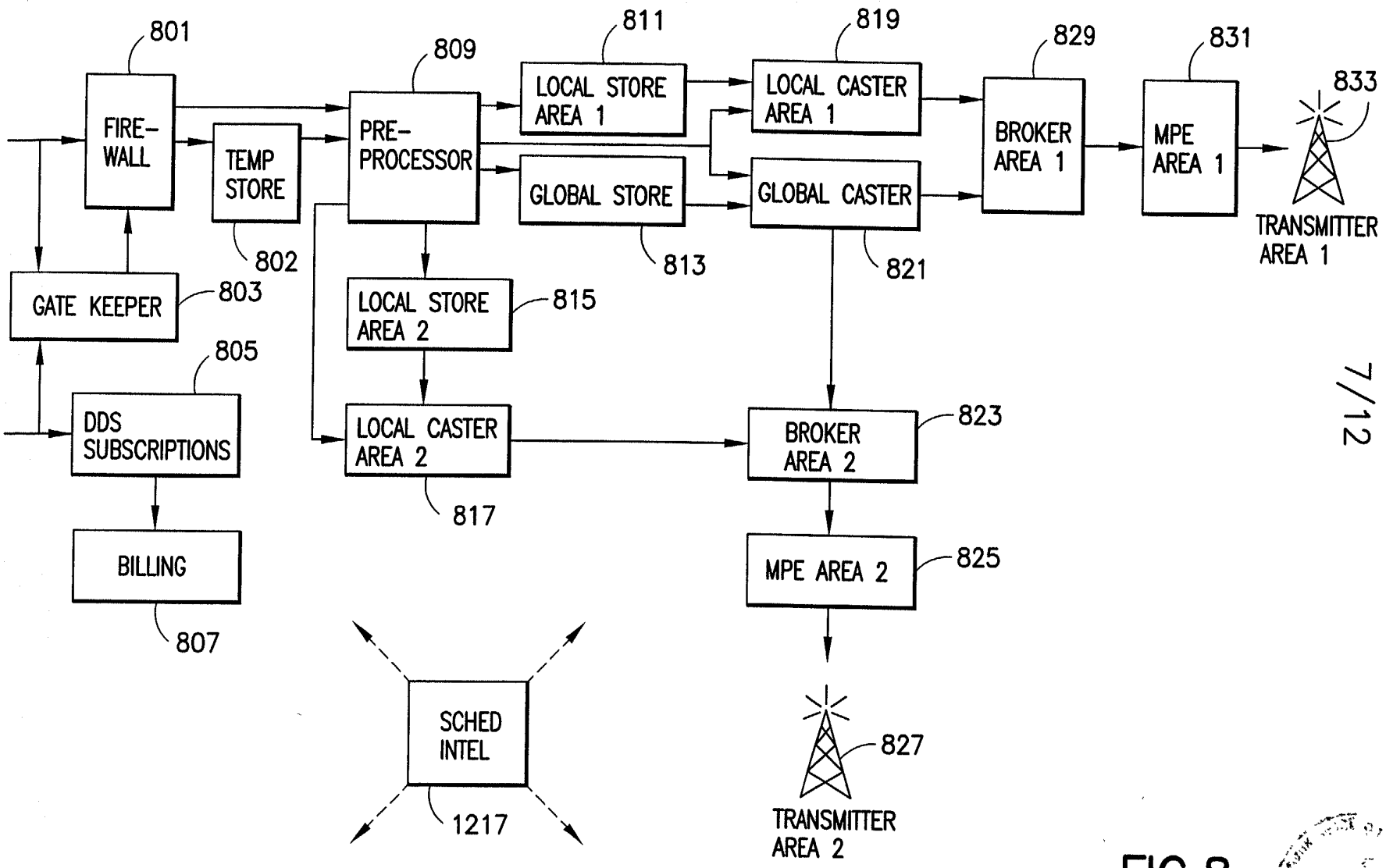
801
FIRE-WALL
TEMP STORE
802
GATE KEEPER
803
805
DDS SUBSCRIPTIONS
BILLING
807
809
PRE-PROCESSOR
811
LOCAL STORE AREA 1
813
GLOBAL STORE
815
LOCAL STORE AREA 2
817
LOCAL CASTER AREA 2
819
LOCAL CASTER AREA 1
821
GLOBAL CASTER
823
BROKER AREA 2
825
MPE AREA 2
827
TRANSMITTER AREA 2
829
BROKER AREA 1
831
MPE AREA 1
833
TRANSMITTER AREA 1
SCHED INTEL
1217

FIG.8

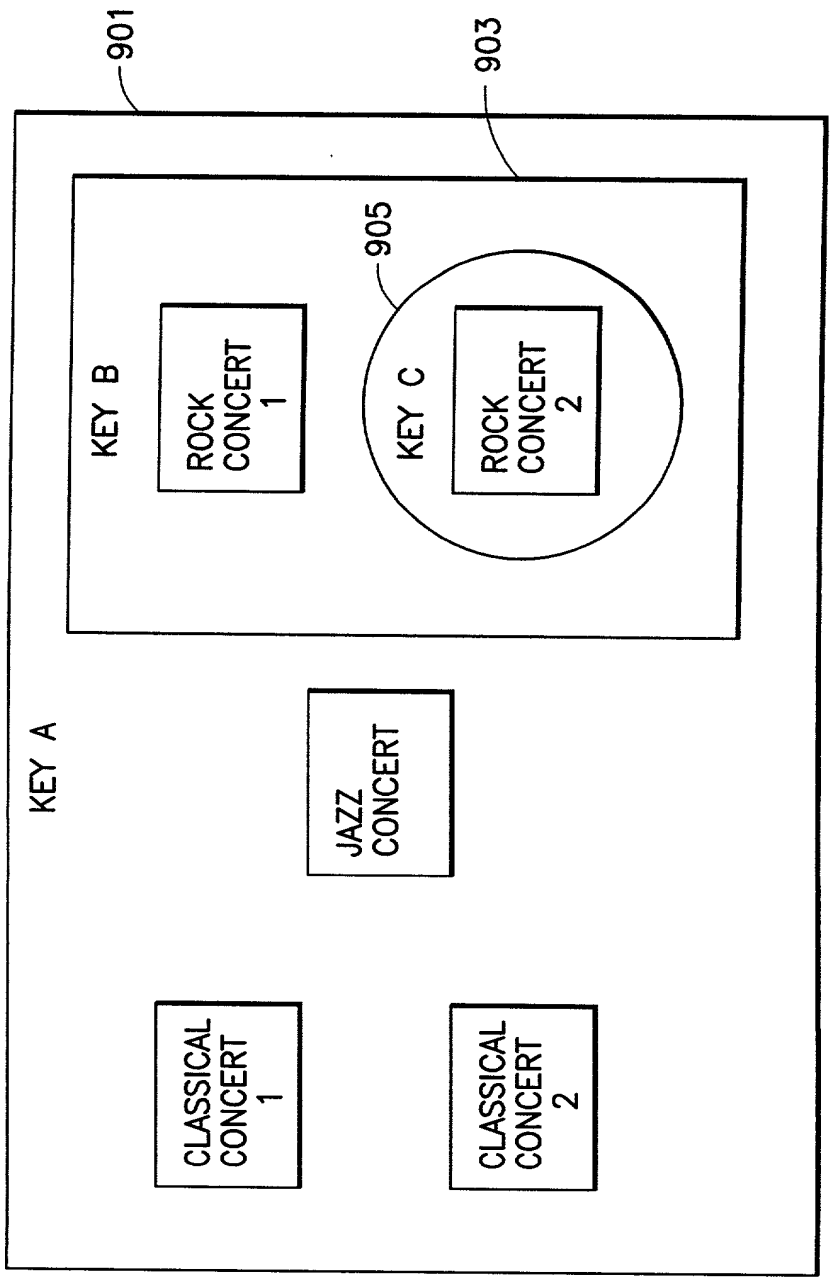
901
903
905
KEY A
KEY B
KEY C
ROCK CONCERT 1
ROCK CONCERT 2
JAZZ CONCERT
CLASSICAL CONCERT 1
CLASSICAL CONCERT 2

FIG.9

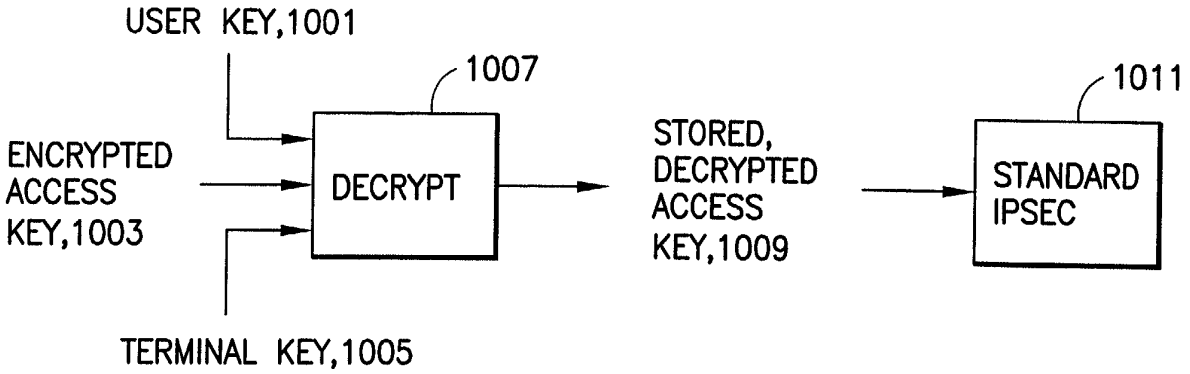
USER KEY,1001
1007
ENCRYPTED ACCESS KEY,1003
DECRYPT
TERMINAL KEY,1005
STORED, DECRYPTED ACCESS KEY,1009
1011
STANDARD IPSEC

FIG.10

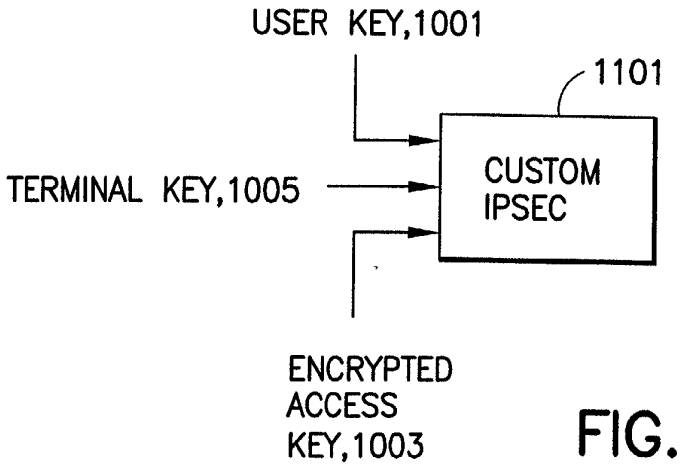
USER KEY,1001
1101
TERMINAL KEY,1005
CUSTOM IPSEC
ENCRYPTED ACCESS KEY,1003

FIG.11

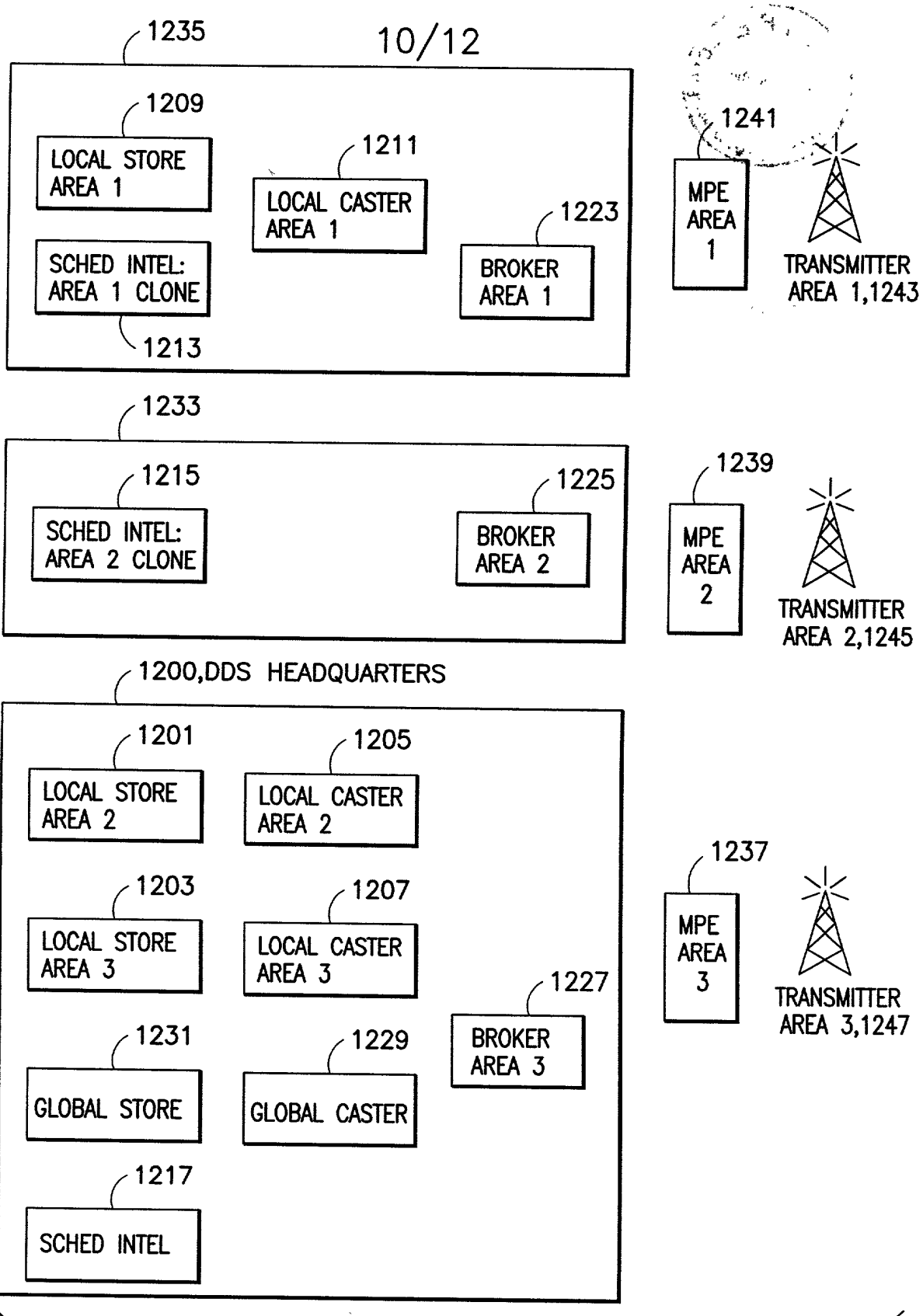
1235
1209
LOCAL STORE AREA 1
1211
LOCAL CASTER AREA 1
1223
BROKER AREA 1
SCHED INTEL: AREA 1 CLONE
1213
1241
MPE AREA 1
TRANSMITTER AREA 1,1243
1233
1215
SCHED INTEL: AREA 2 CLONE
1225
BROKER AREA 2
1239
MPE AREA 2
TRANSMITTER AREA 2,1245
1200,DDS HEADQUARTERS
1201
LOCAL STORE AREA 2
1205
LOCAL CASTER AREA 2
1203
LOCAL STORE AREA 3
1207
LOCAL CASTER AREA 3
1227
BROKER AREA 3
1231
GLOBAL STORE
1229
GLOBAL CASTER
1217
SCHED INTEL
1237
MPE AREA 3
TRANSMITTER AREA 3,1247

FIG.12

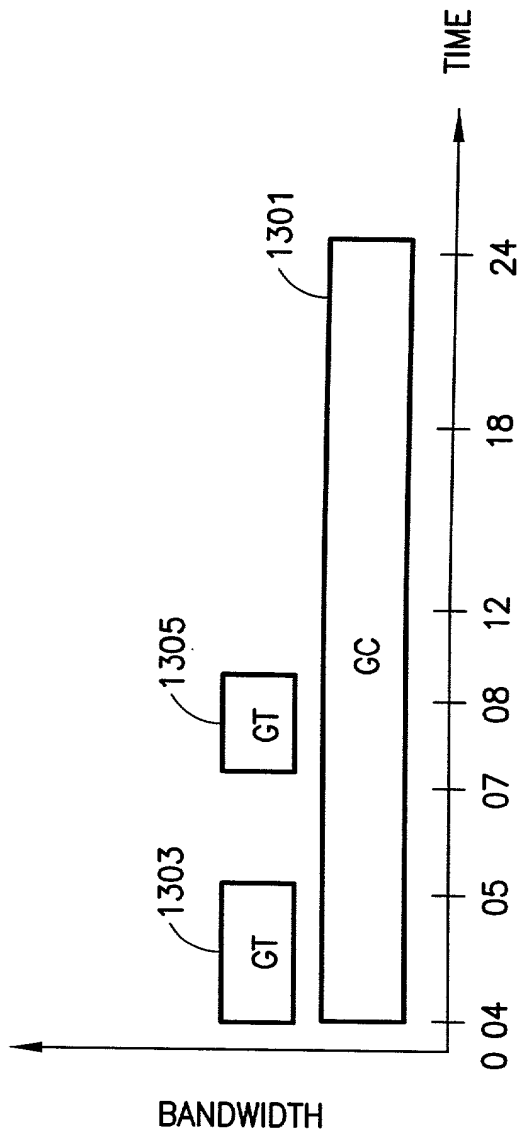

FIG.13

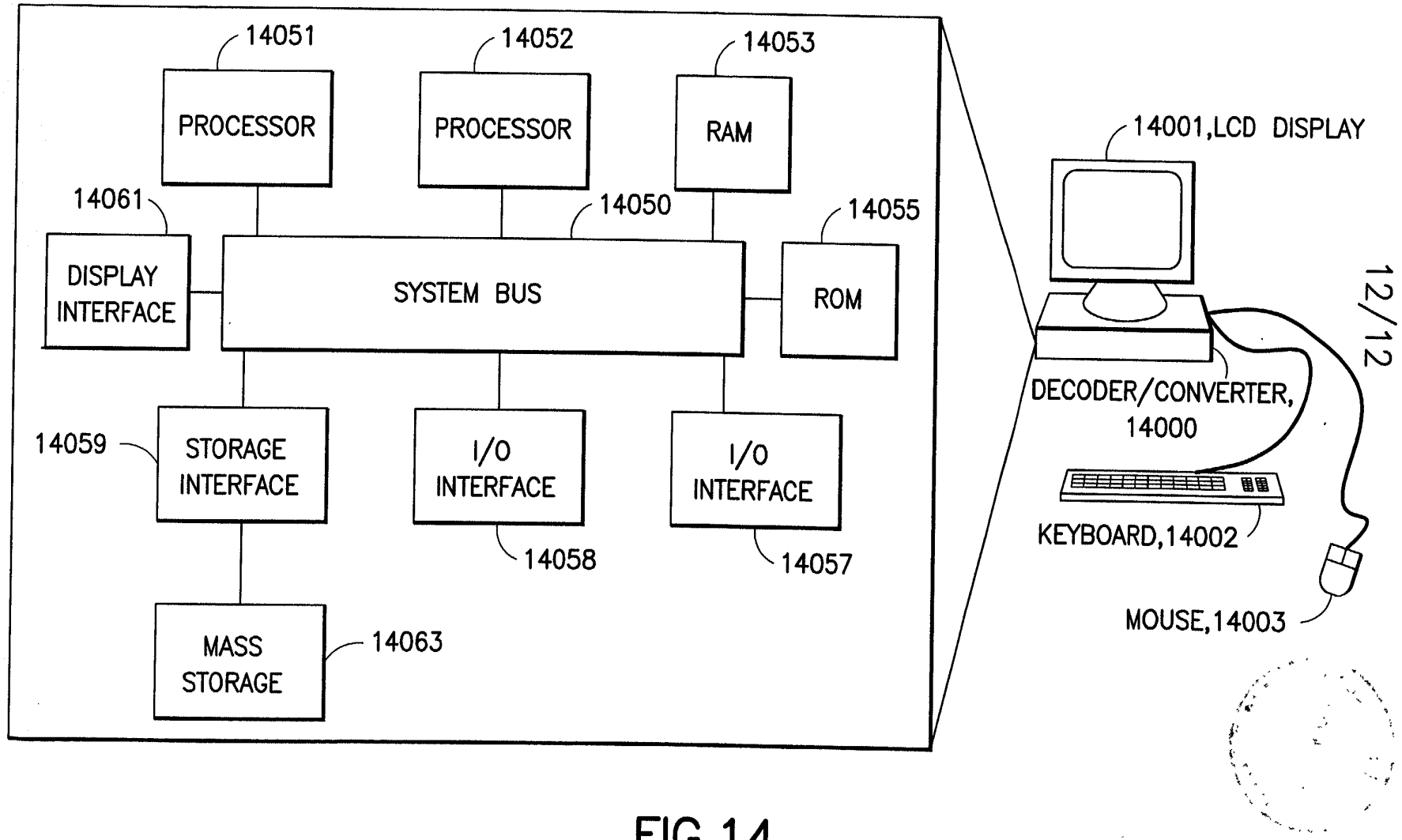
14051
PROCESSOR
14052
PROCESSOR
14053
RAM
14061
DISPLAY INTERFACE
14050
SYSTEM BUS
14055
ROM
14059
STORAGE INTERFACE
I/O INTERFACE
14058
I/O INTERFACE
14057
MASS STORAGE
14063
14001,LCD DISPLAY
DECODER/CONVERTER, 14000
KEYBOARD,14002
MOUSE,14003

FIG.14